

HBM IP Subsystem Implementation: 2.5D ASIC

Open-Silicon



TSMC 2016
Open Innovation Platform®
Ecosystem Forum

ABSTRACT


Access to memory is a critical aspect of successful high-end computing. The conventional approach to memory, where the growing proportion of the total power budget is consumed by memory, has become a limiting factor in overall system performance. Over the last decade, however, high memory bandwidth (HBM) at low power has increased significantly in various high-end computing applications such as graphics. This technology has overcome the prior limitations imposed by conventional memory.

HBM is a technology that ups the bandwidth-per-watt and the bandwidth-per-square-millimeter of die space. It provides high density, low power, low latency, fast flight time and high bandwidth at a lower pin count. HBM gen2 offers 256 GBytePS bandwidth, 8 Gb per die, 2Gbps per pin data rate, and only 2.5-3mw of power consumption per Gbps.

HBM ASIC System-in-Package (SiP) is a fantastic idea, but it presents various challenges with interposer design, die2die IOs, high speed interface, electrical tolerance, assembly of die, mechanical tolerances, ESD, packaging, test and so forth. Hence, the adoption of the 2.5D SiP technology has been slow. During the past several years, 2.5D silicon-interposer based SiP technologies have been proposed and evaluated for ASIC use. Thanks to the advent of JEDEC's, the HBM Gen-2 DRAM standard has advanced significantly. The assembly and manufacturing houses are now addressing many challenges associated with HBM 2.5D SiP. This includes things like the convergence of market needs, a higher memory bandwidth at lower power, and technical capabilities (2.5D Interposer-based ASIC design in combination with the new JEDEC HBM Gen2 standard). It needs the integration of significant capacities of high-bandwidth (up-to 256GB/s for an 8-channel, 8Gb memory stack implementation) and low latency memory inside the ASIC package.


Considering the ever increasing requirement of low power, higher performance and low area, the 16nm FinFet process is the key to HBM subsystem 2.5D ASIC implementation. A 16nm FinFET process can potentially offer a 40-50% performance increase or a 50% power reduction compared to the 28nm process. The complete ecosystem (die, interposer, assembly, packaging) provided by manufacturing and assembly house is very crucial for adaptation of this technology.

During this presentation, Open-Silicon will present its HBM-Gen2 IP in TSMC's 16nm GL "FinFet" process in combination with TSMC's CoWoSTM 2.5D silicon-interposer technology. Aspects to be discussed include the HBM-controller, HBM-PHY and HBM die-to-die interposer-IO implementation, as well as the integration validation of the IP with SK- Hynix's HBM die-stack into a 16nm/2.5D/CoWoSTM ASIC implementation.




Your Idea. Delivered.™

Open-Silicon.com
490 N. McCarthy Blvd, #220
Milpitas, CA 95035
408-245-5700



©Copyright Open-Silicon

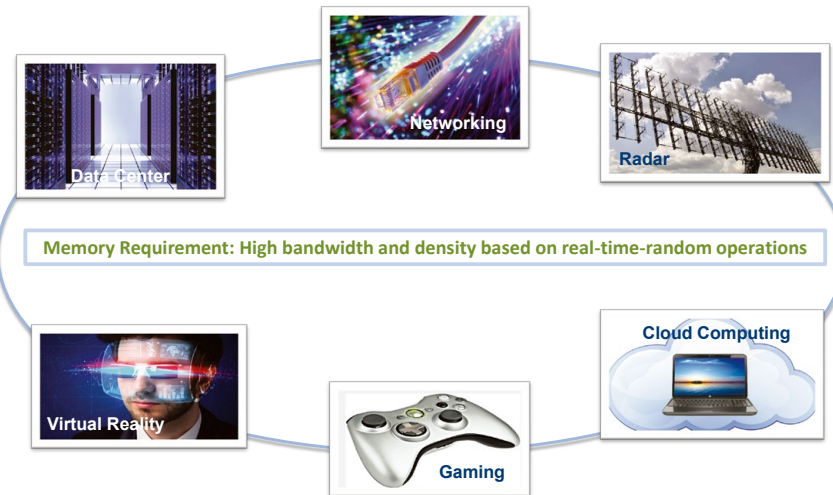


HBM IP Subsystem Implementation: 2.5D ASIC

Bhupesh Dasila
Engineering Manager, Silicon Engineering

Raghuram Jambunathan
Architect, Silicon Engineering

Requirements From Key Applications Form Factor, Bandwidth, Power



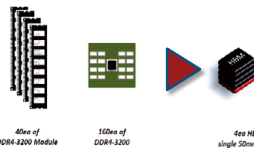
©Copyright Open-Silicon

2

Providing System-Optimized ASIC Solutions

Your Idea. Delivered.™

Key Advantages of High Bandwidth Memory [HBM]

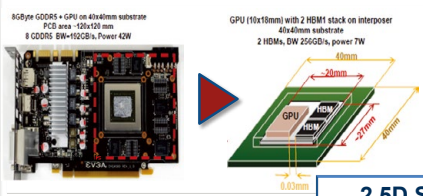


3D Stack

- Multiple independent channels for RD/WR access
- Each channel provides access to independent set of DRAM banks
- Increased active banks with pseudo channel
- Multiple simultaneous access to the memory

Parallelism

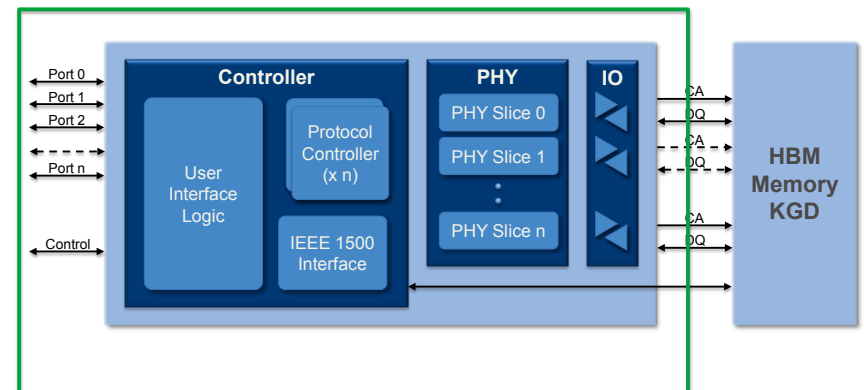
- Semi-independent row and column command interface
- Active traffic along with memory refreshes



2.5D SiP

Protocol Efficiency

HBM IP Subsystem



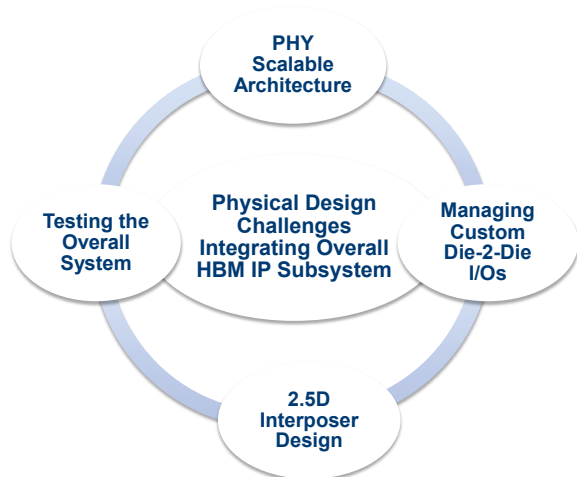
©Copyright Open-Silicon

4

Providing System-Optimized ASIC Solutions

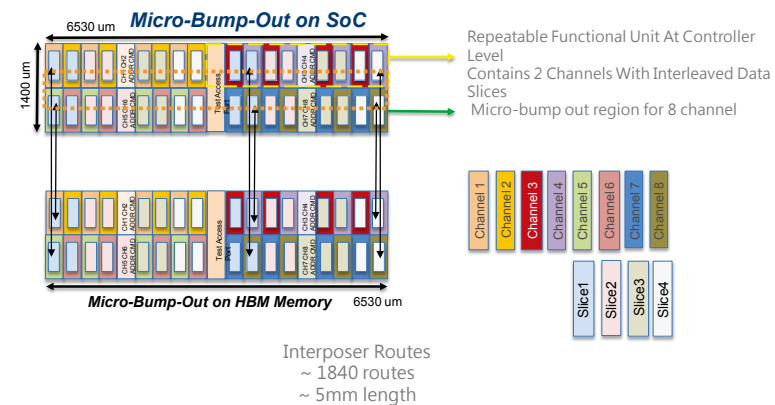
Your Idea. Delivered.™

HBM 2.5D SiP Implementation Challenges



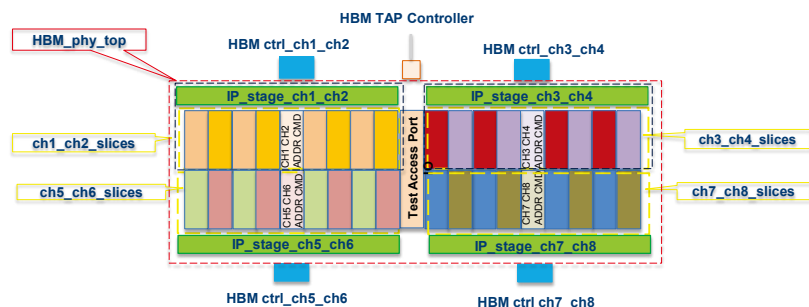
Your Idea. Delivered.™

HBM Memory To Soc Micro-bump-out Interface



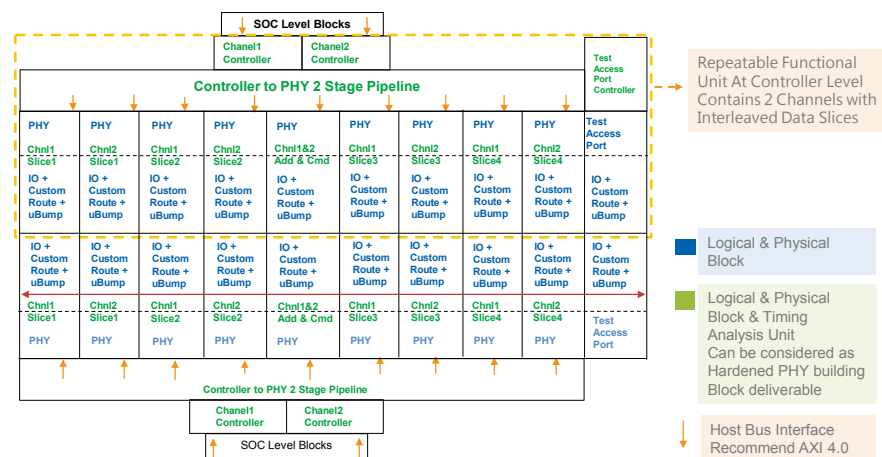
Your Idea. Delivered.

HBM PHY: Physical Hierarchy



Your Idea. Delivered.™

Physical View Of 2 Channel HBM PHY



Your Idea. Delivered.

The diagram illustrates the internal structure of the **rd wr logic module** and its connection to the **HBM IO** and the **Assembled layout view**.

rd wr logic module: This module is responsible for **fifo ctrl and other auto place and route logic**. It contains several logic blocks:

- Wr logic:** Includes **wr logic bit0** and **wr logic bit43**.
- Rd logic:** Includes **rd ffo bit0** and **rd ffo bit43**.
- Wr oen ctrl:** Includes **wr oen ctrl** and **rd ie ctrl**.
- Wr dq:** Includes **wr dq trim dly** and **rd dq trim dly**.
- Wr dq match dly:** Includes **wr dq match dly** and **rd dq match dly**.
- Wr dq clock gating:** Includes **wr dq clock gating**.

The module is connected to the **HBM IO** via **wr dq, dqe, ie & oen buffers to HBM IO**. The **HBM IO** is labeled as **HBM IO + micro-Bump + Custom Route**.

Assembled layout view: This view shows the physical layout of the module, including the **hbm controller**, **buffers**, **pil_dli**, **Pil_dli decap**, **Cmd status reg**, **rd_wr_logic**, and **HBM IO**. The layout is shown in a top-down view, with the **hbm controller** at the top and the **HBM IO** at the bottom.

Figure 1: HBM Memory Bump Array

The figure illustrates the HBM Memory Bump Array, showing a detailed layout view and a corresponding table view.

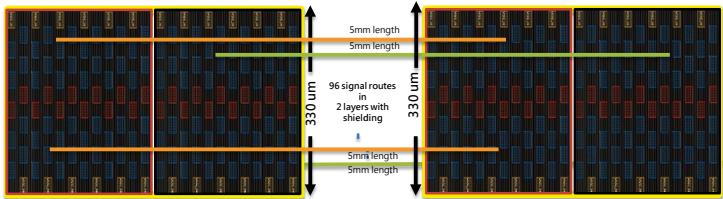
Layout View: The layout shows a grid of memory bumps. Key components labeled include VSS, VSS_E, VSS_S, and U Bump. The array is organized into rows and columns, with specific bumps highlighted in red and yellow.

Table View: The table provides a detailed view of the array structure, showing the layout of the bumps and their connections. The table is organized into rows and columns, with the first column labeled Y and the rest labeled X. The data points are organized into a grid with some cells highlighted in red and others in yellow.

Y	X	331..25	2161.75	2156.25	2161.75	2170.15	2173.75	2186.15	2187.75	2191.15	2193.75	2206.15	2207.75	2210.15	2213.75	2226.15	2227.75	2230.15	2233.75	2246.15	2247.75	2250.15	2253.75	2266.15	2267.75	2270.15	2273.75	2286.15	2287.75	2290.15	2293.75	2306.15	2307.75	2310.15	2313.75	2326.15	2327.75	2330.15	2333.75	2346.15	2347.75	2350.15	2353.75	2366.15	2367.75	2370.15	2373.75	2386.15	2387.75	2390.15	2393.75	2406.15	2407.75	2410.15	2413.75	2426.15	2427.75	2430.15	2433.75	2446.15	2447.75	2450.15	2453.75	2466.15	2467.75	2470.15	2473.75	2486.15	2487.75	2490.15	2493.75	2506.15	2507.75	2510.15	2513.75	2526.15	2527.75	2530.15	2533.75	2546.15	2547.75	2550.15	2553.75	2566.15	2567.75	2570.15	2573.75	2586.15	2587.75	2590.15	2593.75	2606.15	2607.75	2610.15	2613.75	2626.15	2627.75	2630.15	2633.75	2646.15	2647.75	2650.15	2653.75	2666.15	2667.75	2670.15	2673.75	2686.15	2687.75	2690.15	2693.75	2706.15	2707.75	2710.15	2713.75	2726.15	2727.75	2730.15	2733.75	2746.15	2747.75	2750.15	2753.75	2766.15	2767.75	2770.15	2773.75	2786.15	2787.75	2790.15	2793.75	2806.15	2807.75	2810.15	2813.75	2826.15	2827.75	2830.15	2833.75	2846.15	2847.75	2850.15	2853.75	2866.15	2867.75	2870.15	2873.75	2886.15	2887.75	2890.15	2893.75	2906.15	2907.75	2910.15	2913.75	2926.15	2927.75	2930.15	2933.75	2946.15	2947.75	2950.15	2953.75	2966.15	2967.75	2970.15	2973.75	2986.15	2987.75	2990.15	2993.75	3006.15	3007.75	3010.15	3013.75	3026.15	3027.75	3030.15	3033.75	3046.15	3047.75	3050.15	3053.75	3066.15	3067.75	3070.15	3073.75	3086.15	3087.75	3090.15	3093.75	3106.15	3107.75	3110.15	3113.75	3126.15	3127.75	3130.15	3133.75	3146.15	3147.75	3150.15	3153.75	3166.15	3167.75	3170.15	3173.75	3186.15	3187.75	3190.15	3193.75	3206.15	3207.75	3210.15	3213.75	3226.15	3227.75	3230.15	3233.75	3246.15	3247.75	3250.15	3253.75	3266.15	3267.75	3270.15	3273.75	3286.15	3287.75	3290.15	3293.75	3306.15	3307.75	3310.15	3313.75	3326.15	3327.75	3330.15	3333.75	3346.15	3347.75	3350.15	3353.75	3366.15	3367.75	3370.15	3373.75	3386.15	3387.75	3390.15	3393.75	3406.15	3407.75	3410.15	3413.75	3426.15	3427.75	3430.15	3433.75	3446.15	3447.75	3450.15	3453.75	3466.15	3467.75	3470.15	3473.75	3486.15	3487.75	3490.15	3493.75	3506.15	3507.75	3510.15	3513.75	3526.15	3527.75	3530.15	3533.75	3546.15	3547.75	3550.15	3553.75	3566.15	3567.75	3570.15	3573.75	3586.15	3587.75	3590.15	35
---	---	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	---------	----

The diagram illustrates the TSMC Interposer architecture. On the left, a large grey rectangle represents the **HBM Memory**. On the right, a white rectangle represents the **SOC** (System on Chip). A red double-headed arrow labeled **Interposer routes** and **~5mm** connects the HBM Memory to the SOC. The SOC is composed of several vertical blocks: **CTRL BLOCKS** (green), **PHY BLOCKS** (green), **PHY BLOCKS** (dark blue), **PHY BLOCKS** (yellow), **CTRL BLOCKS** (green), and **SOC BLOCKS** (green). The HBM Memory is connected to the SOC via the interposer routes.

Interposer
Single Data Slice Routing



HBM – Memory data slice bump out showing 96 signal bumps

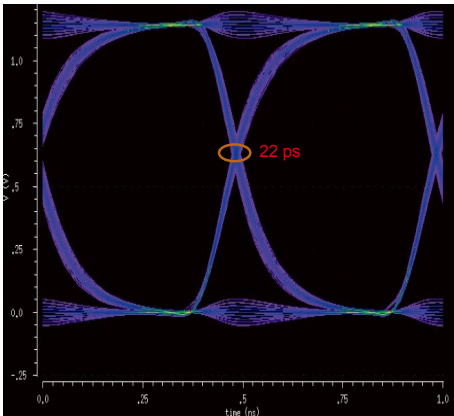
SOC– Data slice bump out showing 96 signal bumps

To effectively shield the signals from any crosstalk, all wires have a ground wire of 0.5 um width, placed at 2.1 um space from signal wire

This leaves a width of 2.1 um per signal wire

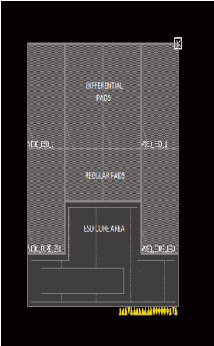
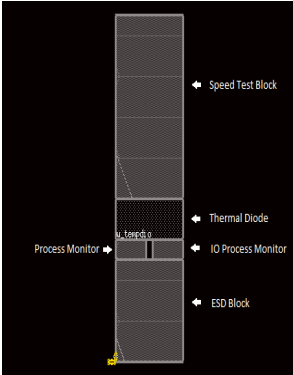
Physical Parameter	Value
Width of signal wire	2.1 um
Length of signal wire	5 mm
Thickness of signal wire	0.85 um
Spacing b/w signal & ground wire	2.1um

Results From Interposer Spice Simulations

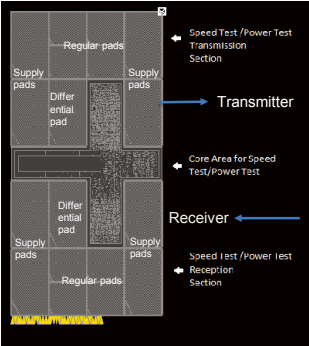


Parameter	Value
RC Delay Model	5 stage pi-network of RC
Driver Model (assumptions)	HBM2 IBIS model as Tx with 18 mA drive operating at minimum corner (125C, 1.14V), 73 ps slew (30% - 70%) at input of the IBIS IO buffer.
Receiver Model	HBM2 IBIS model as Rx operating at maximum corner (for max input cap)
Slew (30% -70%)	90.6 ps
Impact of crosstalk on data window (single corner)	13 ps (no length skew/ocv/input slew or output load variations considered)
Worst Receiver Peak-Peak	1.15 V

HBM PHY Characterization Block



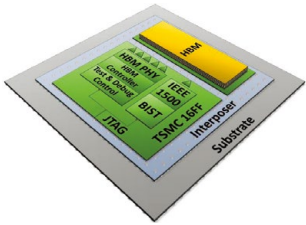
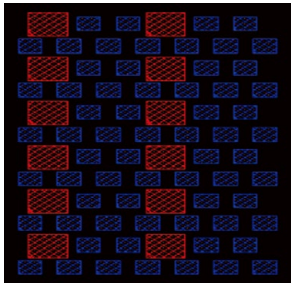
ESD test



Speed test

HBM IP Physical Design for DFT
uBump and Probing

12 Rows and 6 Columns of Micro uBumps Representing a Slice

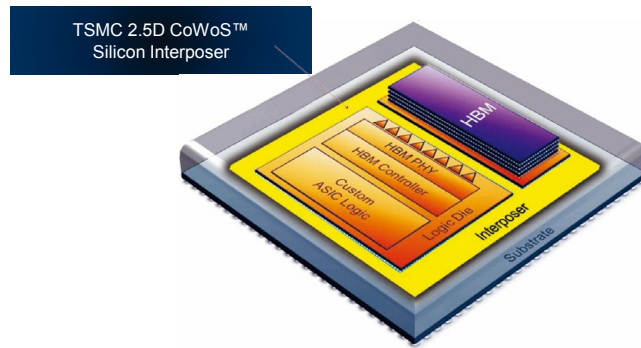


- uBumps
- Probe Pads

Testability feature deployed through probing mechanism for debug of ASIC SiPs with HBM memory embedded on a 2.5D interposer die

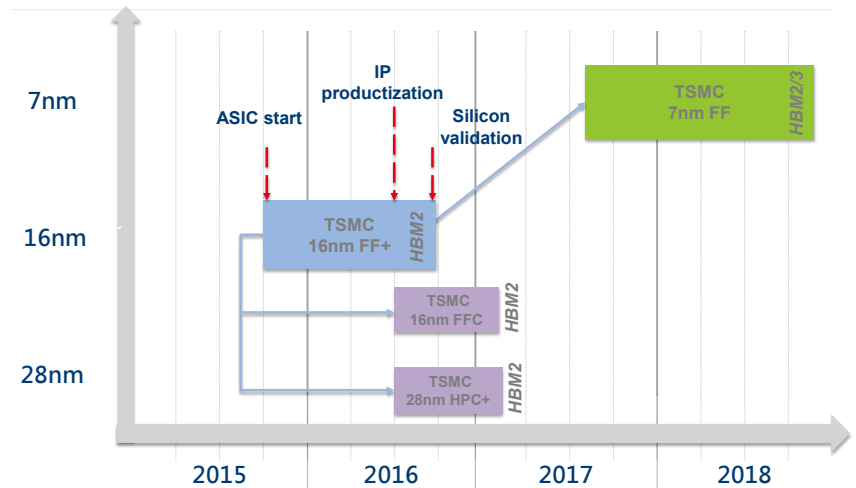
HBM IP Silicon Validation Plans With Lead Demonstration SoC

This Lead SoC Will Demonstrate
IP Subsystem ↔ HBM Die-Stack Interoperability



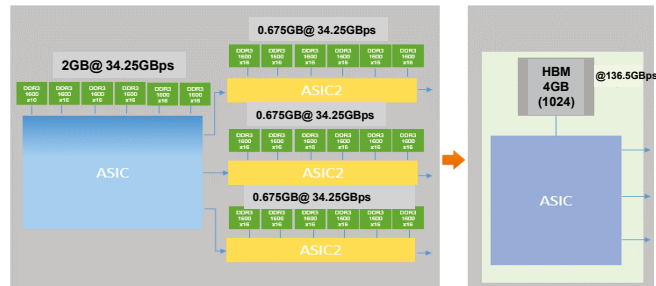
HBM ecosystem is ready for power and form-factor constrained systems in high-performance computing, networking, high-end consumer and graphics applications

HBM IP Subsystem Roadmap TSMC Foundry



System Integration: 2.5D HBM ASIC SiP Solution Lead Customer

Current DDR3 Implementation



HBM Delivers Small Form Factor

	Max. Bandwidth	Power Efficiency
DDR3 (x16)	4 GigaBytes per second	1.00 mW/Gigabits per second/pin
HBM2 (x1024)	256 GigaBytes per second	0.33 mW/Gigabits per second/pin

Summary

- **Full Subsystem IP Solution**
 - HBM Controller + PHY+ IO IP from one source
 - HBM IP subsystem from a single vendor minimizes integration risk
- **Performance**
 - 2Gbps per pin data-rate at longer trace lengths with custom I/O
 - Bandwidth up-to 256GB/s
- **Proven 2.5D ASIC Design and Packaging Experience**
 - Three 2.5D ASIC SiP Designs
 - HBM interface requires a specialized interposer die-to-die IO
- **Testability**
 - Probe pads allow reduced total cost of ownership
 - Loop back allows for issue-isolation for different IP subsystem components
- **Interoperability**
 - HBM 2.5D ASIC Design in progress for lead customer
 - Lead HBM SoC in TSMC 16nm CoWoS™ will demonstrate: IP Subsystem ↔ HBM die-stack interoperability
- **Ecosystem**
 - HBM ecosystem is ready to enable supply of HBM2 ASIC SiPs

